REMARKS

This responds to the Office Action mailed on February 8, 2006, and the references cited therewith.

Claims 1-3 and 5-11 are amended, and new claims 12-16 are added; no claims are canceled. As a result, claims 1-16 are now pending in this application.

§102 Rejection of the Claims

Claim 1 was rejected under 35 U.S.C. § 102(b) for anticipation by Beard et al. (US 5,430,884).

Beard describes an high performance scalar/vector processor. Specifically, Beard describes a method and apparatus for fetching both scalar and vector instructions from an instruction cache in a scalar processing unit, and for controlling the operation of those instructions in both scalar processing units and vector processing units.

Although Beard describes a method and apparatus for controlling dispatch of instructions enabling decoupled operation of the scalar processing unit and the vector processing unit, it does not teach or suggest the particular way of dispatching vector instructions as taught by Applicant and claimed in claim 1.

Applicant, for instance, teaches and claims in claim 1 using a separate vector dispatch unit in the vector processing unit for controlling dispatch of vector instructions for their actual execution. Such an approach is not taught or suggested by Beard.

Furthermore, Beard does not teach or suggest a two-step approach for dispatching vector instructions as described by Applicant and claimed in claim 1. Beard, for example, does not teach or suggest predispatching a vector instruction if the vector instruction is scalar committed as described and claimed by Applicant.

In addition, under Beard's approach, a vector instruction in the vector processing unit is issued for execution if any scalar (or address value) operand is available without waiting for all other required resources are ready. On the contrary, under the invention as claimed in claim 1, a predispatched vector instruction is issued for execution only after all required operands are available.

Claim 1 has been amended to emphasize these differences. Reconsideration is respectfully requested.

It is also indicated by the Examiner that DeLano et al. (USPN 5,787,494) and Nagashima et al. (USPN 4,541,046) are pertinent to applicant's disclosure.

DeLano discloses software-assisted handling of hardware TLB error. Although DeLano is partially relevant to a method and apparatus for handling address translation fault, DeLano does not teach or suggest a multiprocessor system comprising a scalar processing unit and a vector processing unit let alone the two-step dispatch of vector instructions as described and claimed by Applicant.

Although Nagashima discloses a data processing system including both a scalar data processor and a vector data processor, Nagashima, alone or in combination with DeLano, does not teach or suggest the two-step dispatching vector instructions as described and claimed by Applicant. Reconsideration is respectfully requested.

§103 Rejection of the Claims

Claims 2-4 and 7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Beard in view of Patterson et al.

Beard is discussed above.

Patterson describes use of a date cache and an instruction cache along with a register, address translation and dealing with a translation fault, and use of a vector load/store unit in a scalar/vector processing computer system.

Claim 2 is, however, patentable as depending on a patentable base claim. In addition, claim 2 is patentable since none of the cited references, alone or in combination, teach or suggest the translating an address associated with a vector instruction and trapping on a translation fault as described and claimed by Applicant.

Claims 3-4 and 7 are patentable since none of the cited references, alone or in combination, teach or suggest using a load buffer with a two-step approach for dispatching vector instructions as described by Applicant and claimed in claims 3, 4 and 7. As noted at page 3, lines 25-29, by using a load buffer to store data to be transferred to a vector register and by using a two-step approach for dispatching vector instructions, Applicant's invention allows the

computer system to unroll loops dynamically and to get loads started independently for multiple iterations. Claims 3-4 and 7 are patentable since none of the cited references, alone or in combination, teach or suggest decoupling vector data loads from vector instruction execution as described and claimed by Applicant.

Claims 5-6 and 8-9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Beard in view of Gharachorloo et al and/or Patterson.

Beard and Patterson are discussed above.

Gharachorloo describes using buffers for renaming registers.

Claims 5-6 and 8-9 are, however, patentable since none of the cited references, alone or in combination, teach or suggest the two-step approach for dispatching vector instructions as described by Applicant and claimed in claims 5-6 and 8-9. In addition, claims 5-6 are patentable since none of the cited references, alone or in combination, teach or suggest decoupling vector data loads from vector instruction execution through the use of a load buffer as described by Applicant and claimed in claims 5-6. This use of load buffers and vector/scalar unit decoupling permits the dynamic unrolling of loops described above. Furthermore, claims 5-6 are patentable since none of the cited references, alone or in combination, teach or suggest renaming the vector registers as described by Applicant and claimed in claims 5-6.

Claims 10 and 11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Beard and Gharachorloo, further in view of Patterson.

Claims 10 and 11 are, however, patentable since none of the cited references, alone or in combination, teach or suggest using the two-step dispatch of vector instructions in a vector processing unit as described by Applicant and claimed in claims 10-11. In addition, claim 10 is patentable since none of the cited references, alone or in combination, teach or suggest decoupling vector data loads from vector instruction execution through the use of a load buffer as described by Applicant and claimed in claim 10. This use of load buffers and vector/scalar unit decoupling permits the dynamic unrolling of loops described above.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6909 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 1st day of August, 2006.

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